AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A method for improving charge mobility of both NMOS and PMOS devices comprising the steps of:

providing a semiconductor substrate comprising gate structures overlying respective PMOS and NMOS device regions;

forming silicides adjacent the respective gate structures and over an upper portion of the respective gate structures;

forming a first dielectric layer comprising a stress type selected from the group consisting of tensile stress and compressive stress over the respective PMOS and NMOS device regions;

forming a buffer oxide layer overlying the first dielectric layer;

removing a portion of the first dielectric layer overlying one of the PMOS and NMOS device regions;

forming a second dielectric layer comprising a stress type opposite from the first dielectric layer stress type over the respective PMOS and NMOS device regions; and

removing a portion of the second dielectric layer overlying one of the PMOS and NMOS device regions having the underlying first dielectric layer to form a compressive stress dielectric layer over the PMOS device region and a tensile stress dielectric layer over the NMOS device region.

2. (cancelled).

3. (currently amended) The method of claim ~~2~~1, wherein the buffer oxide layer comprises a silicon oxide layer.

4. (currently amended) The method of claim ~~2~~1, wherein the buffer oxide layer is from about 10 Angstroms to about 1000 Angstroms in thickness.

5. (original) The method of claim 1, wherein the first and second dielectric layers comprises a material selected from the group consisting of silicon nitride and silicon oxynitride.

6. (original) The method of claim 1, wherein the first and second dielectric layers are formed by a CVD deposition process selected from the group consisting of LPCVD, ALCVD, and PECVD.

7. (original) The method of claim 6, wherein the first and second dielectric layers are formed by precursors comprising reactants selected from the group consisting of silane (SiH_4), disilane (Si_2H_6), trisilane (Si_3H_8), dichlorosilane (SiH_2Cl_2), trichlorosilane ($SiHCl_3$), hexacholorodisilane (Si_2Cl_6), and mixtures thereof.

8. (original) The method of claim 1, wherein the first and second dielectric layers are from about 10 Angstroms to about 1000 Angstroms in thickness.

9. (original) The method of claim 1, wherein the compressive stress dielectric layer and the tensile stress dielectric layer comprise a stress level up to about 2 GPa.

10. (original) The method of claim 1, wherein the silicide comprises a metal silicide.

11. (original) The method of claim 10 wherein the metal silicide is selected from the group consisting of cobalt silicide and titanium silicide.

12. (original) The method of claim 1, wherein the first and second dielectric layers are formed without a subsequent ion implantation process to relieve a stress level.

13. (original) The method of claim 1, wherein the first and second dielectric layers form a contact etching stop layer in a subsequent damascene formation process.

14. (currently amended) A method for simultaneously improving charge mobility and device drive current of NMOS and PMOS devices comprising the steps of:

providing a semiconductor substrate comprising gate structures and offset spacers overlying respective PMOS and NMOS device regions;

forming source/drain regions;

forming silicides over the source/drain regions and over an upper portion of the respective gate structures;

forming a first dielectric layer comprising a stress type selected from the group consisting of tensile stress and compressive stress over the respective PMOS and NMOS device regions;

<u>forming a buffer oxide layer overlying the first dielectric layer;</u>

removing a portion of the first dielectric layer overlying one of the PMOS and NMOS device regions;

forming a second dielectric layer comprising a stress type opposite from the first dielectric layer stress type over the respective PMOS and NMOS device regions; and

removing the second dielectric layer overlying one of the PMOS and NMOS device regions to form a compressive stress dielectric layer over the PMOS device region and a tensile stress dielectric layer over the NMOS device region.

15. (cancelled).

16. (currently amended) The method of claim ~~15~~<u>14</u>, wherein the buffer oxide layer comprises a silicon oxide layer.

17. (currently amended) The method of claim ~~15~~<u>14</u>, wherein the buffer oxide layer is from about 10 Angstroms to about 1000 Angstroms in thickness.

18. (original) The method of claim 14, wherein the first and second dielectric layers comprise a material selected from the group consisting of silicon nitride and silicon oxynitride.

19. (original) The method of claim 14, wherein the first and second dielectric layers are formed by a CVD deposition process selected from the group consisting of LPCVD, ALCVD, and PECVD.

20. (original) The method of claim 19, wherein the first and second dielectric layers are formed by precursors comprising a reactant selected from the group consisting of silane (SiH_4), disilane (Si_2H_6), trisilane (Si_3H_8), dichlorosilane (SiH_2Cl_2), trichlorosilane ($SiHCl_3$), hexacholorodisilane (Si_2Cl_6), and mixtures thereof.

21. (original) The method of claim 14, wherein the first and second dielectric layers are from about 10 Angstroms to about 1000 Angstroms in thickness.

22. (original) The method of claim 14, wherein the compressive stress dielectric layer and the tensile stress dielectric layer comprise a stress level up to about 2 GPa.

23. (original) The method of claim 14, wherein the silicides comprise a metal silicide selected from the group consisting of cobalt silicide and titanium silicide.

24. (original) The method of claim 14, wherein the first and second dielectric layers are formed without a subsequent ion implantation process to relieve a stress level.

25. (original) The method of claim 1, wherein the first and second dielectric layers form a contact etching stop layer in a subsequent damascene formation process.

26-39. (cancelled).

40. (currently amended) A method for manufacturinga semiconductor device, comprising:

providing a semiconductor substrate comprising a first gate structure overlying a PMOS device region and a second gate structure overlying a NMOS device region;

forming a first layer with first stress over the NMOS region;

<u>forming a buffer oxide layer overlying the first layer;</u> and

forming a second layer with second stress over the PMOS region such that an interface is formed between the first layer and the second layer;

wherein the second stress is different from the first stress.